UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,913	03/18/2004	Hiroshi Suzuki	1309.43669X00	5412
24956 7590 12/21/2007 MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C. 1800 DIAGONAL ROAD SUITE 370 ALEXANDRIA, VA 22314			EXAMINER	
			AMRANY, ADI	
			ART UNIT	PAPER NUMBER
			2836	
			MAIL DATE	DELIVERY MODE
			12/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

, ·				
	Application No.	Applicant(s)		
	10/802,913	SUZUKI ET AL.		
Office Action Summary	Examiner	Art Unit		
	Adi Amrany	2836		
The MAILING DATE of this communication Period for Reply	n appears on the cover sheet wi	ith the correspondence address		
A SHORTENED STATUTORY PERIOD FOR R WHICHEVER IS LONGER, FROM THE MAILIN - Extensions of time may be available under the provisions of 37 C after SIX (6) MONTHS from the mailing date of this communication - If NO period for reply is specified above, the maximum statutory of the same of the period for reply within the set or extended period for reply will, by - Any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).	IG DATE OF THIS COMMUNION FR 1.136(a). In no event, however, may a ron. Seriod will apply and will expire SIX (6) MON statute, cause the application to become AB	CATION. reply be timely filed  NTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).		
Status				
1) Responsive to communication(s) filed on	26 November 2007.			
2a) ☐ This action is <b>FINAL</b> . 2b) ☑	This action is <b>FINAL</b> . 2b)⊠ This action is non-final.			
3) Since this application is in condition for all	lowance except for formal matt	ers, prosecution as to the merits is		
closed in accordance with the practice un	der <i>Ex parte Quayle</i> , 1935 C.D	). 11, 453 O.G. 213.		
Disposition of Claims				
4) Claim(s) <u>1-8,11,15-19 and 21-31</u> is/are pe	ending in the application.	·		
4a) Of the above claim(s) is/are wit	_	•		
5) Claim(s) <u>1-8,11,15,16,18 and 19</u> is/are all	owed.			
6)⊠ Claim(s) <u>17 and 21-31</u> is/are rejected.	•			
7) Claim(s) is/are objected to.				
8) Claim(s) are subject to restriction a	and/or election requirement.			
application Papers		·		
9) The specification is objected to by the Exa	miner.			
10) The drawing(s) filed on is/are: a)	accepted or b) objected to	by the Examiner.		
Applicant may not request that any objection to	o the drawing(s) be held in abeyar	nce. See 37 CFR 1.85(a).		
Replacement drawing sheet(s) including the co	orrection is required if the drawing	(s) is objected to. See 37 CFR 1.121(d).		
11) The oath or declaration is objected to by the	ne Examiner. Note the attached	d Office Action or form PTO-152.		
riority under 35 U.S.C. § 119				
12)⊠ Acknowledgment is made of a claim for for a)⊠ All b)□ Some * c)□ None of:	reign priority under 35 U.S.C. §	§ 119(a)-(d) or (f).		
1. Certified copies of the priority docu				
2. Certified copies of the priority docu				
3. Copies of the certified copies of the	•	received in this National Stage		
application from the International B	•	ivad		
* See the attached detailed Office action for	a list of the certified copies not	received.		
Attachment(s)	_			
) Notice of References Cited (PTO-892)		Summary (PTO-413) s)/Mail Date		
<ul> <li>Notice of Draftsperson's Patent Drawing Review (PTO-94</li> <li>Information Disclosure Statement(s) (PTO/SB/08)</li> </ul>		nformal Patent Application		
Paper No(s)/Mail Date 11/27/07.	6) 🔲 Other:	<del></del>		

10/802,913 Art Unit: 2836

## **DETAILED ACTION**

## Response to Arguments

1. Although previous office actions indicated the allowability of claim 17, upon further consideration, a new ground of rejection is made in view of the previously cited references, namely Penny, which discloses said main body comprises different types of storage device packs (see fig 7).

## Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 17 and 21-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oomori (US 2004/0003306) in view of Mizuno (US 5,838,891), Penny (US 2003/0199515) and Adapted FS4500 to SATA RAID (IDS 2/9/07, item AS).

With respect to claim 17, Oomori discloses a storage system (fig 1, item 11; par 18) comprising:

a power supply circuit (21) which outputs a single type of power having a single voltage level (210; par 22-24);

a main body (11) having a main power supply line (210-110) to transmit said single type of power output from said power supply circuit, a data transfer path for data transfer (motherboard connecting 112 and 114; par 20), and a plurality of pack connection sites (connection of 114 to motherboard); and

Art Unit: 2836

a plurality of storage device packs (114) which can receive power from said main body, which are each connected to said plurality of pack connection sites on said main body so as to enable exchange of date with said data transfer path;

wherein said data transfer path of said main body forms a first data transfer interface (inherent, as this limitation only names an existing transfer path).

At the time of the invention by applicants, it would have been to one skilled in the art to configure the Oomori single type of power to be equal to or higher than the highest voltage level of said one or more types of power required by said physical storage devices, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2s 272, 205 USPQ 215 (CCPA 1980).

Oomori does not expressly disclose:

A. each storage device pack comprises a physical storage device and a power conversion circuit. Oomori discloses the power conversion circuit (117) is located external to and shared by all of the storage device packs.

- B. said plurality of storage device packs connected to said pack connection sites on said main body comprises different types of storage device packs, comprising first and second types.
- C. said first and second type of storage device comprises a first/second type of physical storage device having a first data transfer interface; and a power conversion

10/802,913 Art Unit: 2836

circuit to convert said single power into power required by said first type of physical storage device.

D. said second type of storage device comprises a data transfer interface conversion circuit.

A. Mizuno discloses that each storage device pack (fig 3) comprises a physical storage device (unnumbered disk) and a power conversion circuit (item 6) which converts said single type of power into one or more types of power required by said physical storage device units (col. 6, lines 56-59; col. 8, lines 14-24). Oomori and Mizuno are analogous because they are from the same field of endeavor, namely power supplies for computer storage systems. At the time of the invention by applicants, it would have been obvious to one skilled in the art to modify the Oomori storage system by placing the DC/DC converter within the housing of each storage device in order to allow the DC/DC converter to be specifically tailored to the corresponding storage device.

B. Penny discloses the storage device packs comprise different types of storage device packs (fig 7, items 710-718; par 33-34). Oomori, Mizuno and Penny are analogous because they are from the same field of endeavor, namely RAID systems. At the time of the invention by applicants, it would have been obvious to one skilled in the art to combine the Oomori and Mizuno power systems with the Penny FC/SATA storage system in order to support a plurality of storage device packs (Penny, abstract).

10/802,913 Art Unit: 2836

said plurality of storage device packs connected to said pack connection sites on said main body comprises different types of storage device packs, comprising first and second types.

- C. Mizuno further discloses that each storage device comprises a physical storage device having a data transfer interface (fig 3, 6, connection to back plane) and a power conversion circuit (DC/DC converter) to convert said single power into power required by each type of physical storage device.
- D. Penny further discloses that said second type of storage device (712) comprises a data transfer interface conversion circuit (par 25 and 33-34).

Adaptec also discloses a data transfer interface conversion circuit (par 2).

Oomori, Mizuno, Penny and Adaptec are analogous because they are from the same field of endeavor, namely RAID systems. At the time of the invention by applicants, it would have been obvious to one skilled in the art to combine the Oomori, Mizuno and Penny storage systems with the Adaptec FC/SATA converter in order to allow the Penny SATA device to properly communicate with the FC host computer (Adaptec, par 1).

With respect to claim 21, Penny discloses at least one of said physical storage devices is a FC storage device (710) and at least another one of said physical storage devices is a SATA storage device (712), wherein said storage device pack having a SATA storage device also includes a FC/SATA converter (par 33). Mizuno discloses the power conversion circuit is coupled to all of the internal circuits of the physical storage device (col. 8, lines 20-24).

10/802;913 Art Unit: 2836

With respect to claim 22, it would be obvious to configure the Mizuno first power conversion circuit supplies power via a single power supply line. The number of supply lines is determined by the configuration of internal circuits.

With respect to claim 23, Oomori discloses said power supply circuit is aAC/DC power supply (fig 1, item 21; par 22). Mizuno discloses said power conversion circuit is a DC/DC converter. It would be obvious to configure said first voltage value to be higher than said single voltage value (Mizuno converter is a buck converter), since the output of the converter is determined by the configuration of the storage device circuitry.

With respect to claim 24, Mizuno discloses said physical storage devices incorporate internal voltage conversion circuits, as discussed above.

With respect to claim 25, Mizuno discloses power having one of the plurality of voltage values converted by said internal voltage conversion circuits is used to drive magnetic storage media of said physical storage devices, and power having another of said plurality of voltage values is used to drive interface logic circuit of said physical storage devices (col. 8, lines 20-24).

With respect to claim 26, Mizuno discloses said first voltage converter receives power one voltage value, as discussed above.

With respect to claim 27, Mizuno discloses:

wherein any of said plurality of storage device packs is a first storage device pack (fig 6; topmost disk enclosure) having a first power conversion circuit; and

10/802,913 Art Unit: 2836

wherein any of the other of said plurality of storage device packs is a second storage device pack (fig 6; nth disk enclosure) having a second power conversion circuit.

It would be obvious to one skilled in the art to configure the plurality of Mizuno DC/DC converters to output a different voltage level, as determined by the associated storage device because the Mizuno converter is designed to supply power to all of the storage device's internal components.

With respect to claim 28, Oomori further discloses a motherboard is positioned between said first power supplies and said housings, and said first voltage converter is connected, via said motherboard, to a power supply line connecting said storage device. Mizuno also disclose a motherboard (fig 6, item 9).

With respect to claim 29, the first paragraph is a repeat of the limitations of claim 17 (top of page 10), and the remaining limitations have been rejected, as discussed above in the rejection of claim 21.

With respect to claim 30, Oomori discloses a control circuit (fig 1, item 112; par 19), and further discloses that each power conversion circuit comprises regulators (par 39). It would be obvious to one skilled in the art that the Oomori system comprises a power supply control circuit which individually controls the turning-on and turning-off of said power conversion circuits. At the time of the invention by applicants, it would have been obvious to combine the control circuit disclosed in Oomori with the internal conversion circuits disclosed in Mizuno in order to supply the correct amount of power (full vs zero) to the storage devices.

10/802,913 Art Unit: 2836

With respect to claim 31, and as discussed above, Oomori discloses a control circuit and that each power conversion circuit comprises regulators. It would be obvious to one skilled in the art that the Oomori system comprises a power supply control circuit which individually controls the output voltage levels of said power conversion circuits according to the power supply voltage levels required by each of said physical storage devices within said plurality of storage device packs. At the time of the invention by applicants, it would have been obvious to combine the control circuit disclosed in Oomori with the internal conversion circuits disclosed in Mizuno in order to supply the correct amount of power to the storage devices.

## Allowable Subject Matter

4. Claims 1-8, 11 and 15-16 are allowed, as these claims all depend from claim 15, which is allowable as indicated in the Non-Final Rejection (July 21, 2006).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adi Amrany whose telephone number is (571) 272-0415. The examiner can normally be reached on Mon-Thurs, from 10am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800 x36. The fax phone

Art Unit: 2836

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA

SUPLIFICATION OF THE SAME LET THE STATE OF THE SAME LET T